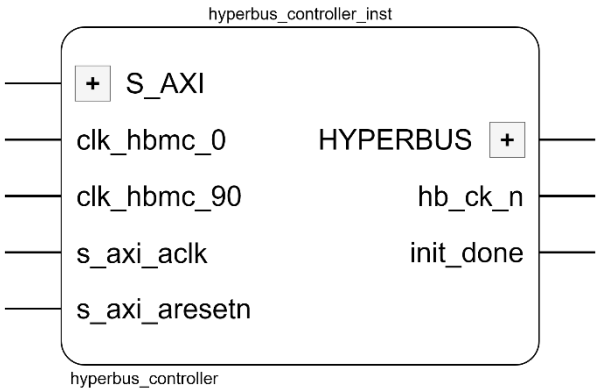
Hyperbus™ controller v2.0

Overview:

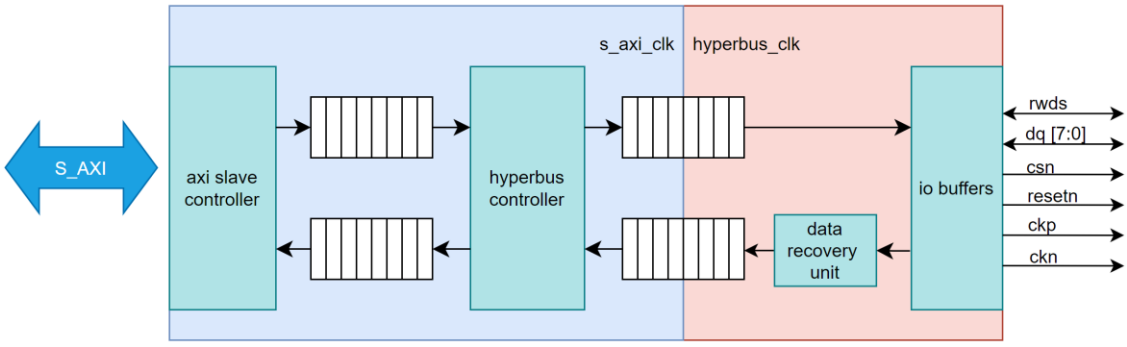


Citrobits' HyperRAM™ memory controller was strategically designed with user accessibility as a top priority, leveraging the AXI 4 interface, widely adopted in modern system architectures. This design choice ensures effortless integration into existing systems, aligning with industry standards and simplifying development processes. Additionally, the controller offers self-calibration delay to facilitate users to operate with the IP. Moreover, another parameters can be set through generics, empowering them to tailor the controller's operation to their specific requirements. The controller is capable of operating at speeds of up to 200MHz, providing a realistic and reliable solution for a diverse range of memory-intensive tasks.

Block diagram:

The block diagram illustrates the connections between the different IP blocks. First, the AXI slave controller will parse the user request. The information will flow to the Hyperbus™ controllers by means of two FIFOs that act as frame buffers in case of congestion. The Hyperbus™ controller contains the required logic to perform the operations over the memory. There are two FIFOS to perform the clock domain crossing between AXI and Hyperbus™.

In Hyperbus™ clock domain, there is the data recovery unit, which synchronizes the received data from the physical pins. Finally, the io buffers, that instantiate the buffers and the required delays to the signals.



CITROBITS

Features:

- Configurable Generics for initial Hyperbus™ configuration
  - Drive Strength
  - CS Timming
- Read Write operations through AXI4-MM
  - AXI4 clock must be *greater or equal* to half the Hyperbus™ clock frequency
- AXI4-MM interface 32b, 64b
  - 128b planned for future releases
- No delay configuration needed for operation frequency of 10-50 MHz
- Automatic optimal delay setting (This can enabled by asserting a generic)
- 200MHz Hyperbus™ support.
  - Configurable IODELAY for optimum sampling point (up to 3.2 ns delay)

Resource Utilization (Certus-NX):

Fixed delay:

LUT4 Logic	LUT4 Distributed RAM	LUT4 Ripple Logic	PFU Registers	IO Buffers	DSP Mult	EBR
714	0	248	927	13	0	7

Calibration engine enabled:

LUT4 Logic	LUT4 Distributed RAM	LUT4 Ripple Logic	PFU Registers	IO Buffers	DSP Mult	EBR
1185	96	494	1296	11	0	8